In the Abstract:

~~Method for fabricating a short channel field-effect transistor~~

~~The invention relates to a method for fabricating a short channel field-effect transistor, comprising the steps of: forming a sublithographic gate sacrificial layer (3M), forming spacers (7S) at the side walls of the gate sacrificial layer (3M), removing the gate sacrificial layer (3M) to form a gate recess and forming a gate dielectric (10) and a control layer (11) in the gate recess. The result is a short channel FET with minimal fluctuations in the critical dimensions in a range below 100 nanometers.~~

A method for fabricating a short channel field-effect transistor is presented. A sublithographic gate sacrificial layer is formed, as are spacers at the side walls of the gate sacrificial layer. The gate sacrificial layer is removed to form a gate recess and a gate dielectric and a control layer are formed in the gate recess. The result is a short channel field-effect transistor with minimal fluctuations in the critical dimensions in a range below 100 nanometers.